LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Currently Amended) A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench, said first gate region continuous in a lateral direction parallel to said surface;

implanting a buffer region beneath said first gate; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region, and wherein said second gate region is continuous in said lateral direction and is narrower than said first gate region.

16. (Original) The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said first gate.

17. (Original) The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said buffer region.

18. (Original) The method of Claim 15, further comprising forming a sidewall spacer to establish a width of said second gate.

19. (Original) The method of Claim 15, further comprising annealing said substrate subsequent to implanting said second gate.

20. (Original) The method of Claim 15, further comprising annealing said substrate after said implanting said second gate.